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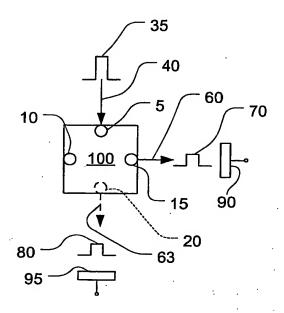


Fig. 1a

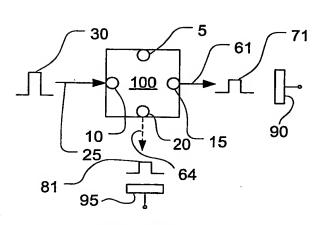


Fig. 1b

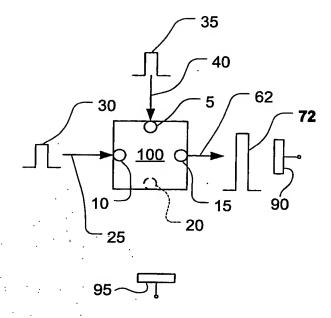


Fig. 1c

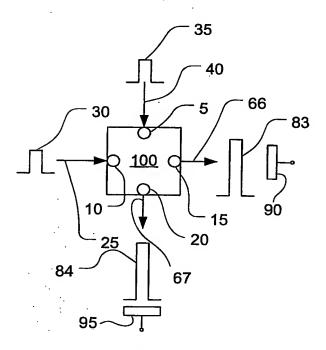
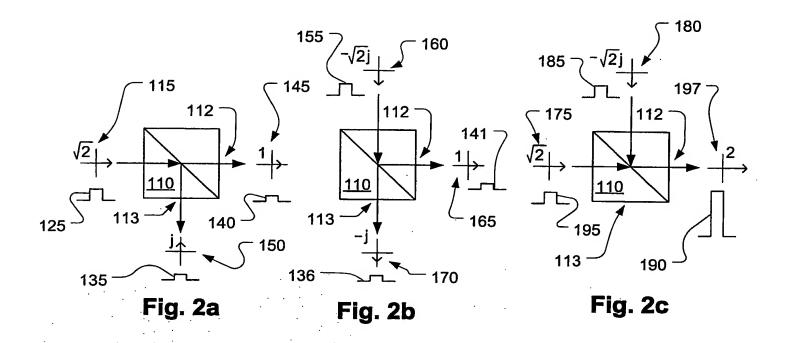
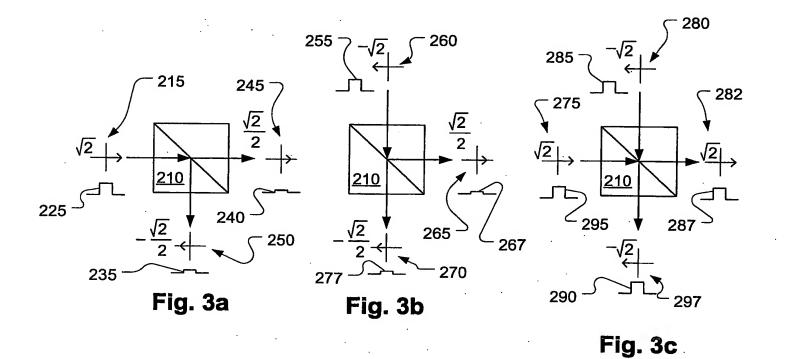
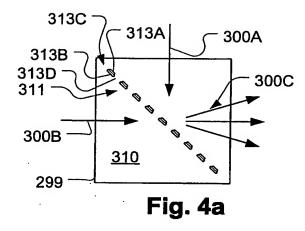
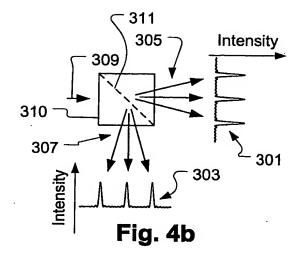


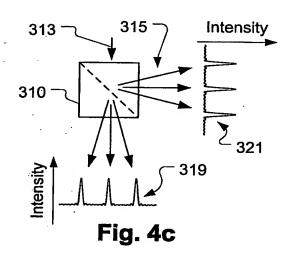
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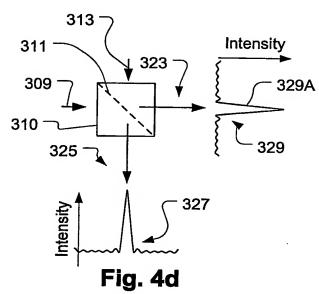


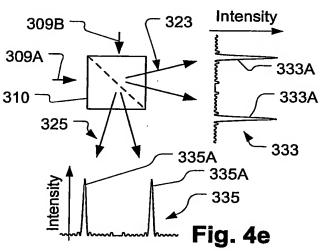












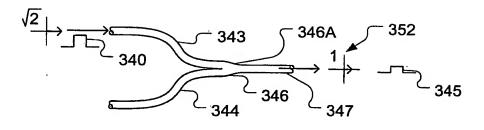
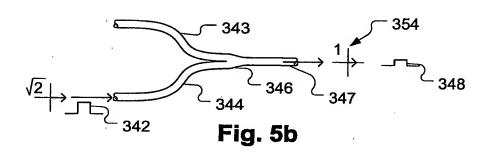
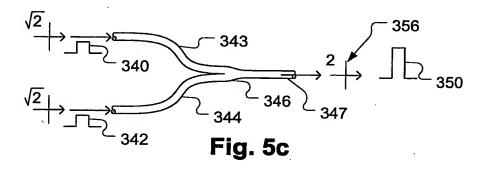


Fig. 5a





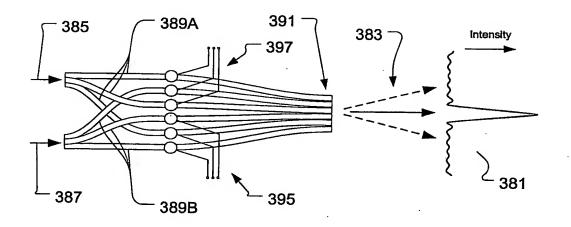


Fig. 7a

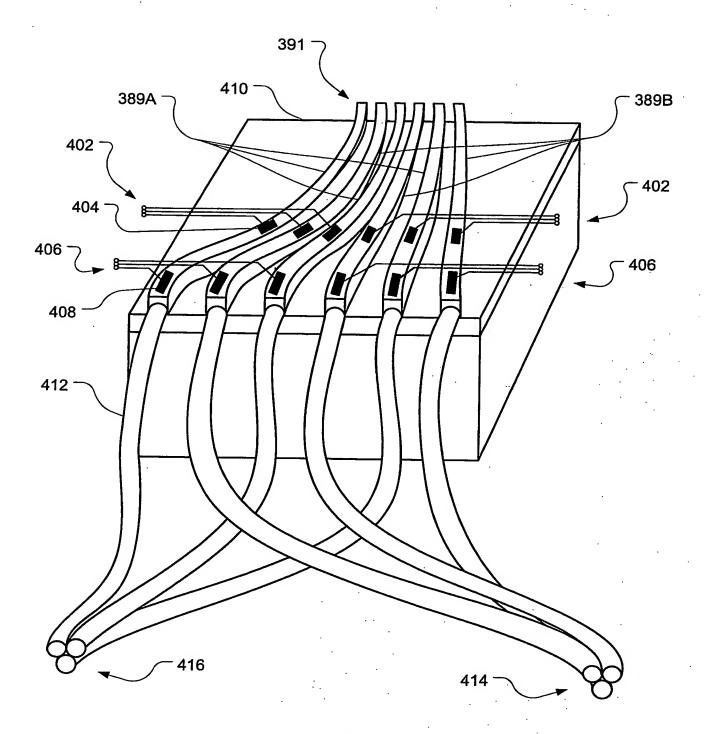
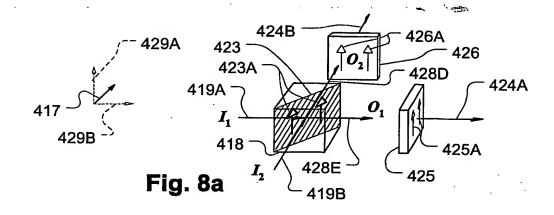
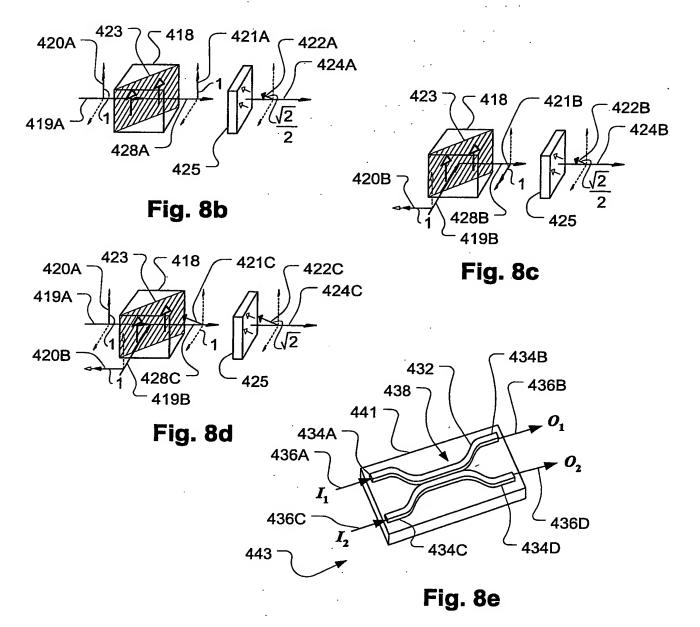


Fig. 7b





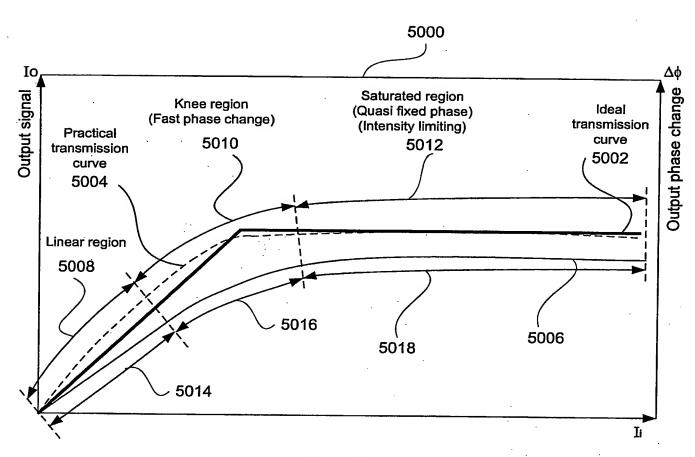


Fig. 9a

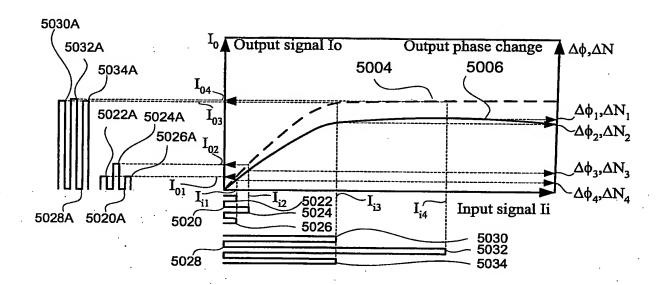


Fig. 9b

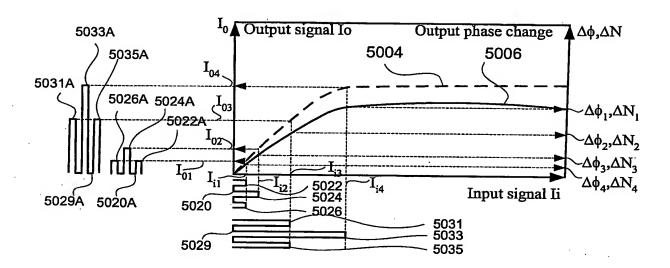


Fig. 9c

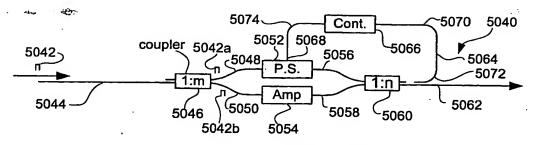
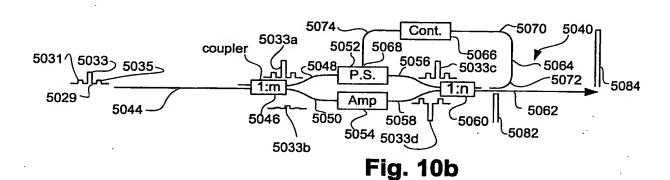


Fig. 10a



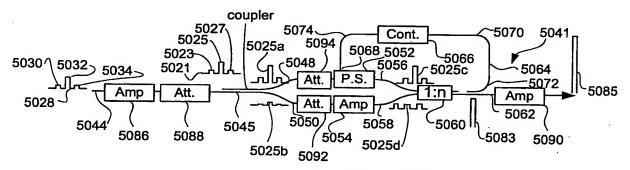
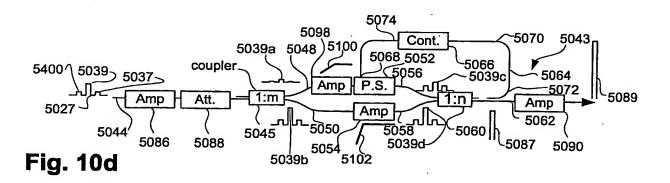
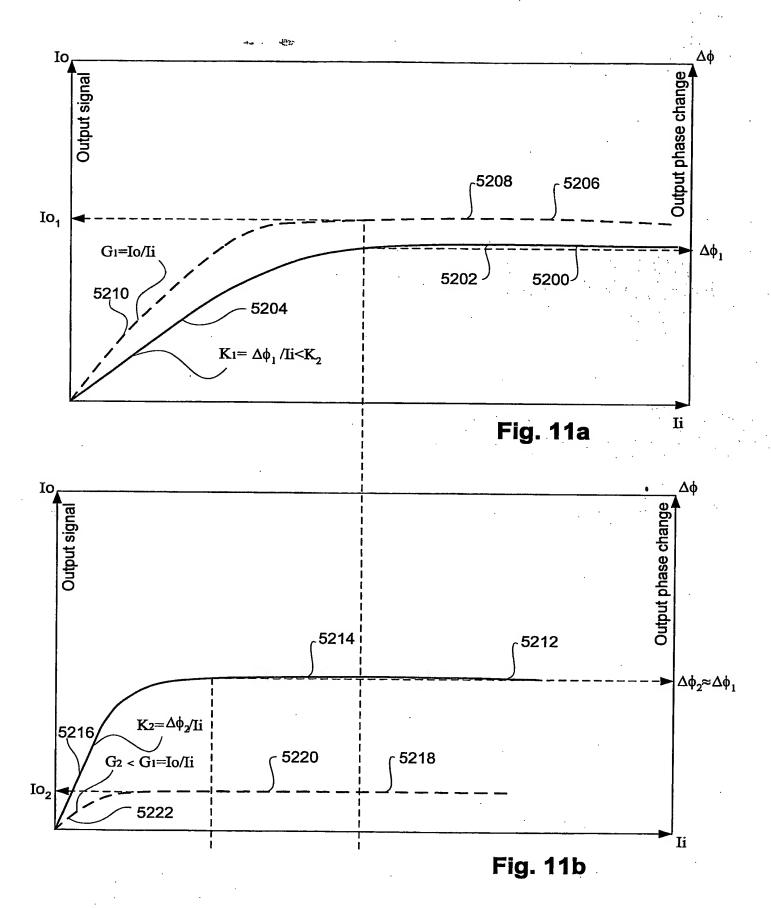
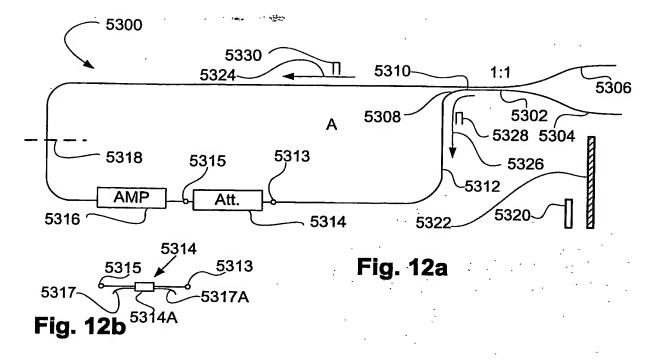


Fig. 10c







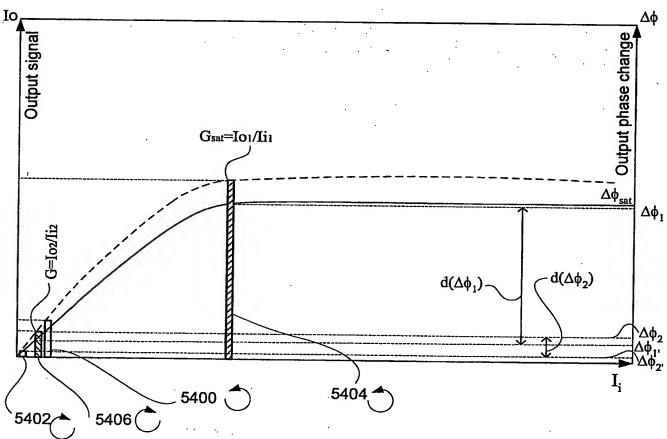


Fig. 13

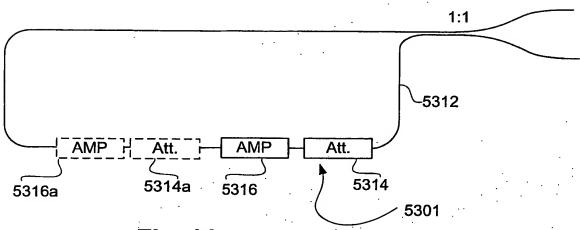


Fig. 14

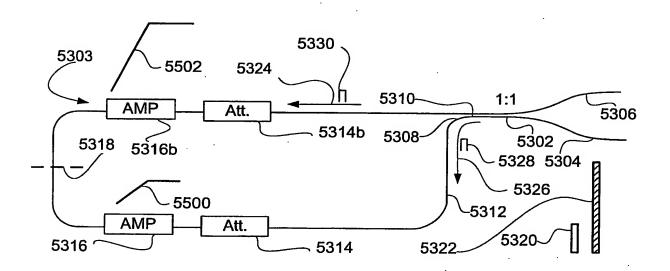
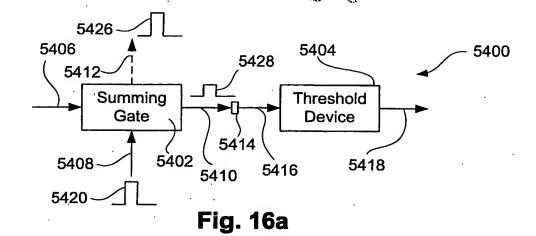
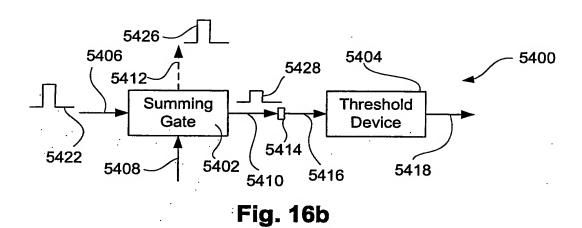


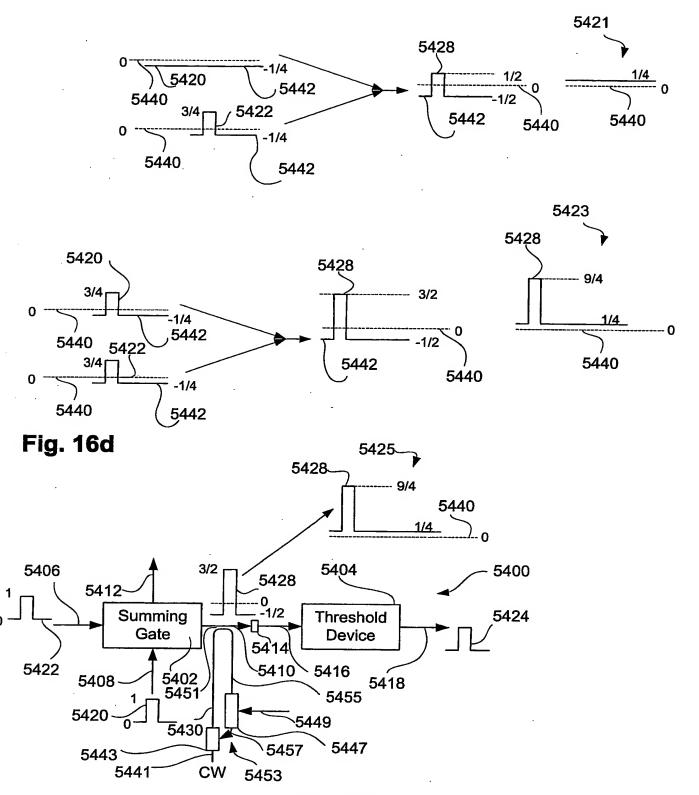
Fig. 15





Summing Threshold Gate Device 5410 5416

Fig.16c



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Fig. 16e

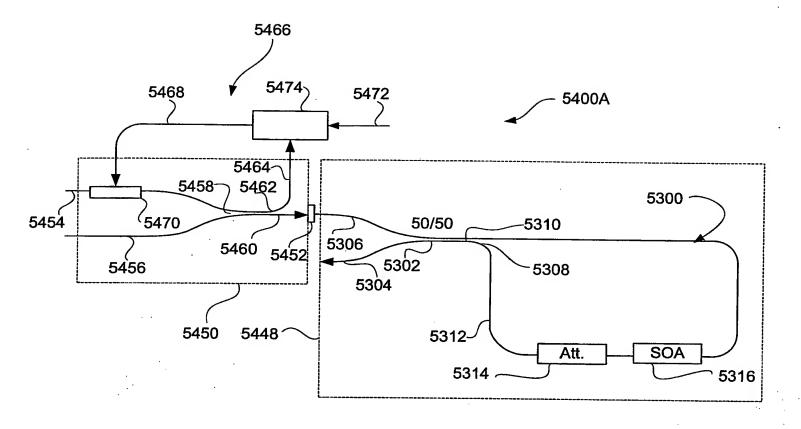
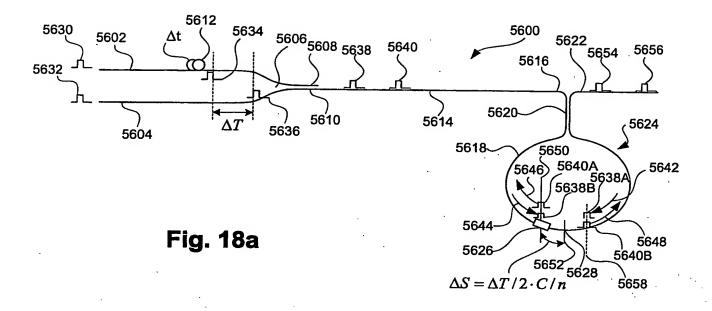
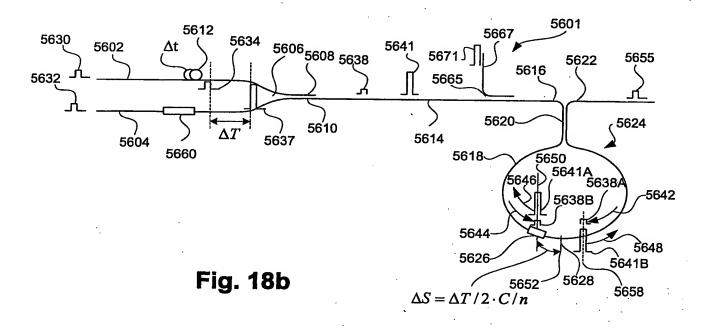


Fig.17





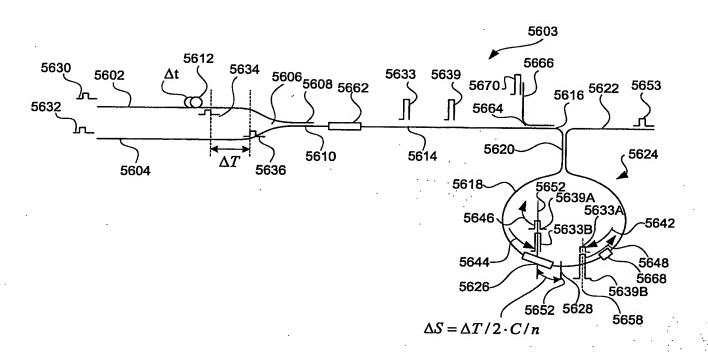


Fig. 18c

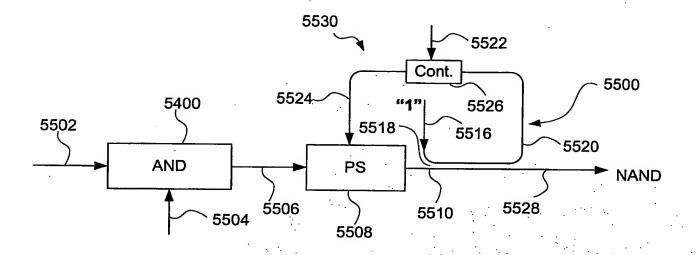


Fig. 19a

